Code No: A5711 **NR**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, October/November-2011
MODELLING AND SYSTHESIS WITH VERILOG HDL
(VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1. Explain the two basic styles of behavioral description in Verilog giving examples. [12]

2. Explain the sequential user-defined primitives describing level-sensitive and edge-sensitive behavior and give examples. [12]

3. (a) Explain the different operators available in Verilog HDL.
   (b) Briefly explain the predefined Verilog data types for nets and registers. [12]

4. Explain the salient features of the following procedural continuous assignment,
   (i) assign…deassign, (ii) force…release. [12]

5. (a) Explain the synthesis of edge-triggered flip flops.
   (b) Summarise the key differences between Verilog descriptions of explicit and implicit finite state machines. [12]

6. (a) Explain the synthesis of any one counter using Verilog.
   (b) List out various elements that may be included within a Verilog model. [12]

7. (a) Discuss why switch-level modeling is useful.
   (b) Explain the Verilog model of a three-input static CMOS NAND gate with the help of a diagram. [12]

8. Write short notes on any two of the following:
   (a) Synthesis of priority structures
   (b) Disable statement and fork…join statement
   (c) Benefits of HDL based designs. [12]

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